

Positive Preannouncements, RTEC Analyst Day

Positive Preannouncements: GSIT actually preannounced expected 4Q *upside* after the close yesterday thanks to Cisco and military customers. Revenue 3Q was \$16.0M, original 4Q guidance was -6-0%, and yesterday's preannouncement called for \$17.5M or +9.4%. Cisco is growing to \$6.5m from \$4.9M. Finally, some good news.

Also, last Thursday Dialog Semiconductor in Germany (and not in my Universe) preannounced expected 4Q revenue of \$268M up from original guidance of \$215-235M due to strength from smart phones and tablets, and for which Apple is a major customer that could account for some half of total sales. Interesting data point especially after yesterday's WSJ report of Apple cutting orders to suppliers. Strong 4Q/Weak 1Q? Dialog is presenting at the Needham conference this morning at 10am, although is unlikely to offer much insight prior to earnings on Feb 20.

Also, LLTC kicks-off earnings season after the close with a press release, then a call Wed at 11:30am ET.

RTEC Analyst Day: Rudolf Technologies (RTEC) hosted an analyst day in NYC yesterday. While I can't comment on fundamental valuation for this semiconductor equipment supplier beyond the scope of my current Universe, I can opine that I am impressed with its strategy to serve advanced packaging markets with its collection of equipment offerings—especially following its very recent acquisition of Azores' lithography tools.

RTEC makes metrology and inspection tools and software. Basically it measures and inspects semiconductor chips at the wafer level. In front-end, or wafer fab operations, its tools measure the thickness of an oxide or metal layer to confirm the processing step occurred as intended. And its software collects and digests data from these measurements and inspections to help identify and trouble-shoot any problems or inconsistencies that may be occurring in the manufacturing environment. Back-end, or package assembly and test operations, also use the inspection tools when they receive wafers from the fab to help them characterize and confirm what they are receiving before die is cut from the wafer and packaged. Inspection tools and software are used in both front-end (fab) and back-end (package assembly) operations, while metrology (measurement) tools are only used in front-end operations. While revenue splits between front-end and back-end customers vary from quarter to quarter, RTEC is well established and serves both fairly equally in terms of revenue over longer periods of time.

Front-end fabs make wafers that consist of dozens or hundreds (sometime thousands) of die, and back-end operations cut the die from the wafer and wrap packages around them (to protect the die from the very dirty real world) and add leads so the die can connect to some other electronic circuit in the very dirty real world. Sometimes two or more die are put into a package where they are connected together internally, and this is usually called a module. Chip-scale packages are not much bigger than the die themselves (hence the name), and bumps are used instead of finger-like leads for connections because they take up less space.

Current advanced packaging goes beyond packages and modules and uses all kinds of crazy schemes to piggy-back die (sometimes in packages, sometimes not) on top of each other in order to fit all the chips required in a tiny cell phone to make it work. These piggy-backing, 'advanced packaging' schemes are forcing back-end operations to deal with smaller and smaller leads and bumps—and now the bumps are being added onto die while they are still on the wafer. Advanced packaging has become a confusing situation where back-end operations are now processing bumps and other kinds of connections at the wafer level. And the tiny size of these bumps and other connection types need lithography tools to create the patterns—tools that used to only be found in front-end, wafer fab operations.

But don't confuse these back-end litho tools that make tiny bumps, with front-end litho tools that make even tinier lines on chips that make those tiny bumps look like planets. Yes they are both lithography tools, but the size and scale and cost are many orders of magnitude different. The RTEC acquisition of Azores gives it back-end lithography tools that Azores has mostly been selling to flat panel display manufacturers, and that RTEC has been jointly working to modify for back-end semiconductor use since 2010.

The bad news is that advanced packaging operations are somewhat blurring the former distinction between front-end and back-end semiconductor operations. But the good news for RTEC is that it has always been dealing in both, and now has a set of metrology, inspection, software and (now) lithography (*back-end* lithography) tools that is uniquely positioned to serve emerging advanced packaging requirements. And this market has a +35% CAGR.

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